UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/661,037 | 09/12/2003 | John D. Hyde | IMPJ-0003D1 | 6704 |

7590 08/25/2004

David B. Ritchie
Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640

| EXAMINER | |
|---|---|
| SOWARD, IDA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/661,037 | HYDE ET AL. | |
| | Examiner | Art Unit | |
| | Ida M Soward | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *36-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36,37,39 and 40* is/are rejected.

7)☒ Claim(s) *38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-26-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the preliminary amendment filed September 12, 2003.

### *Specification*

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36-37 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diorio et al. (5,990,512) in view of Alavi et al. (5,844,300).

In regard to claim 36, Diorio et al. teach a pFET synapse transistor 32, comprising: a p- doped substrate; a first n- well (left well) and a second n- well (right well) disposed in the substrate; a first p+ doped region disposed in the first n- well (left well) forming a source (left p+ region) and a second p+ doped region disposed in the first n- well (left well) forming a drain (right p+ region); a channel disposed in the first n- well (left well) between the source (left p+ region) and the drain (right p+ region); a

tunneling junction in the second n- well (right well); a layer of gate oxide 50 disposed above the channel, the first n- well (left well) and the second n- well (right well); a polysilicon floating gate 44 disposed above the layer of gate oxide 50; source contact terminal electrically coupled to the source (left p+ region); a drain contact terminal electrically coupled to the drain (right p+ region); a well contact terminal coupled to the second n- well (right well) (Figures 7A-7B, columns 10-11, lines 37-67 and 1-30, respectively).

In regard to claim 39, Diorio et al. teach the transistor formed with a single layer of conductive polysilicon 44 (Figures 7A-7B, columns 10-11, lines 37-67 and 1-30, respectively).

However, Diorio et al. fail to teach a third p+ doped region and a fourth p+ doped region disposed in a second well.

In regard to claim 36, Alavi et al. teach a third p+ doped region and a fourth p+ doped region disposed in a second well 41 (Figure 3, column 4, lines 40-67).

In regard to claim 37, Alavi et al. teach the third p+ doped region and the fourth p+ doped region (in n- well 41) shorted together with a conductive layer 60 which forms a bridge over a floating gate (Figure 3, columns 4-5, lines 40-67 and 17-25, respectively).

In regard to claim 40, Alavi et al. teach the transistor fabricated using a CMOS process. Also, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90

(209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113.

Since Diorio et al. and Alavi et al. are from the same field of endeavor (pFET transistors), the purpose disclosed by Alavi et al. would have been recognized in the pertinent art of Diorio et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the pFET synapse transistor structure as taught by Diorio et al. with the structure having third and fourth p+ doped regions disposed in a second well as taught by Alavi et al. to develop a structure capable of monitoring electrostatic charge (col. 1, lines 8-10).

### *Allowable Subject Matter*

Claim 38 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to pFET semiconductor devices:

Atsumi et al. (5,438,542)

Bergemont (US 6,563,731 B1)

Furuhata et al. (US 6,294,427 B1)

Gogoi et al. (US 2002/0072144 A1)

Smayling et al. (5,204,541).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
August 20, 2004

Michael Trinh
Primary Examiner
Act SPE